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SCLCI04M01

BLE module (SIP)

(Preliminary)

V1.5

Revision History

Date	Revision Content	Revised By	Version
2022/06/21	- Initial released		1.5
	-		
	-		
	-		
	-		

Contents

1. FEATURES

MainChip:

Bluetooth® 5, IEEE 802.15.4-2006, 2.4 GHz transceiver

- -95 dBm sensitivity in 1 Mbps Bluetooth® low energy mode
- -103 dBm sensitivity in 125 kbps Bluetooth® low energy mode (long range)
- -20 to +8 dBm TX power, configurable in 4 dB steps
- On-air compatible with nRF52, nRF51, nRF24L, and nRF24AP
- Series Supported data rates:
  - Bluetooth® 5 – 2 Mbps, 1 Mbps, 500 kbps, and 125 kbps
  - IEEE 802.15.4-2006 – 250 kbps
  - Proprietary 2.4 GHz – 2 Mbps, 1 Mbps
- Single-ended antenna output (on-chip balun)
- 128-bit AES/ECB/CCM/AAR co-processor (on-the-fly packet encryption)
- 4.8 mA peak current in TX (0 dBm)
- 4.6 mA peak current in RX
- RSSI (1 dB resolution)

ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz

- 212 EEMBC CoreMark® score running from flash memory
- 52 µA/MHz running CoreMark from flash memory
- Watchpoint and trace debug modules (DWT, ETM, and ITM)
- Serial wire debug (SWD)

Rich set of security features

- ARM® TrustZone® Cryptocell 310 security subsystem
  - NIST SP800-90A and SP800-90B compliant random number generator
  - AES-128 – ECB, CBC, CMAC/CBC-MAC, CTR, CCM/CCM*
  - Chacha20/Poly1305 AEAD supporting 128- and 256-bit key size
  - SHA-1, SHA-2 up to 256 bits
  - Keyed-hash message authentication code (HMAC)
  - RSA up to 2048-bit key size
  - SRP up to 3072-bit key size
  - ECC support for most used curves, including P-256 (secp256r1) and Ed25519/Curve25519
  - Application key management using derived key model

Secure boot ready

- Flash access control list (ACL)

- Root-of-trust (RoT)
- Debug control and configuration
- Access port protection (CTRL-AP)

Secure erase

Flexible power management

- 1.7 V to 3.6 V supply voltage range
- Automated peripheral power management
- Fast wake-up using 64 MHz internal oscillator
- 0.4 µA at 3 V in System OFF mode, no RAM retention
- 1.5 µA at 3 V in System ON mode, no RAM retention, wake on RTC

1 MB flash and 256 kB RAM

Advanced on-chip interfaces

- USB 2.0 full speed (12 Mbps) controller
- QSPI 32 MHz interface
- High-speed 32 MHz SPI
- Type 2 near field communication (NFC-A) tag with wake-on field
  - Touch-to-pair support
- Programmable peripheral interconnect (PPI)
- 48 general purpose I/O pins
- EasyDMA automated data transfer between memory and peripherals

Nordic SoftDevice ready with support for concurrent multiprotocol
12-bit, 200 ksps ADC – 8 configurable channels with programmable gain
64 level comparator
15 level low-power comparator with wake-up from System OFF mode
Temperature sensor
4x four channel pulse width modulator (PWM) unit with EasyDMA
Audio peripherals – I2S, digital microphone interface (PDM)
5x 32-bit timer with counter mode
Up to 4x SPI master/3x SPI slave with EasyDMA
Up to 2x I2C compatible two-wire master/slave
2x UART (CTS/RTS) with EasyDMA
Quadrature decoder (QDEC)
3x real-time counter (RTC)
Single crystal operation

Flash:

16M-bit Serial Flash

- 2048K-Byte
- 256 Bytes per programmable page

Standard, Dual, Quad SPI

- Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
- Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#
- Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3

High Speed Clock Frequency

- 133MHz for fast read with 30PF load
- Dual I/O Data transfer up to 266Mbits/s
- Quad I/O Data transfer up to 532Mbits/s

Software/Hardware Write Protection

- Write protect all/portion of memory via software
- Enable/Disable protection with WP# Pin
- Top/Bottom Block protection

Endurance and Data Retention

- Minimum 100,000 Program/Erase Cycles
- 20-year data retention typical

Allows XiP (eXecute in Place) Operation

- High speed Read reduce overall XiP instruction fetch time
- Continuous Read with Wrap further reduce data latency to fill up SoC cache

Fast Program/Erase Speed

- Page Program time: 0.4ms typical
- Sector Erase time: 45ms typical
- Block Erase time: 0.15s/0.25s typical
- Chip Erase time: 6s typical

Flexible Architecture

- Uniform Sector of 4K-Byte
- Uniform Block of 32/64K-Byte

Low Power Consumption

- 11μA typical standby current
- 1μA typical deep power down current

Advanced Security Features

- 128-bit Unique ID for each device
- Serial Flash Discoverable parameters (SFDP) register 2x1024-
- Byte Security Registers With OTP Locks

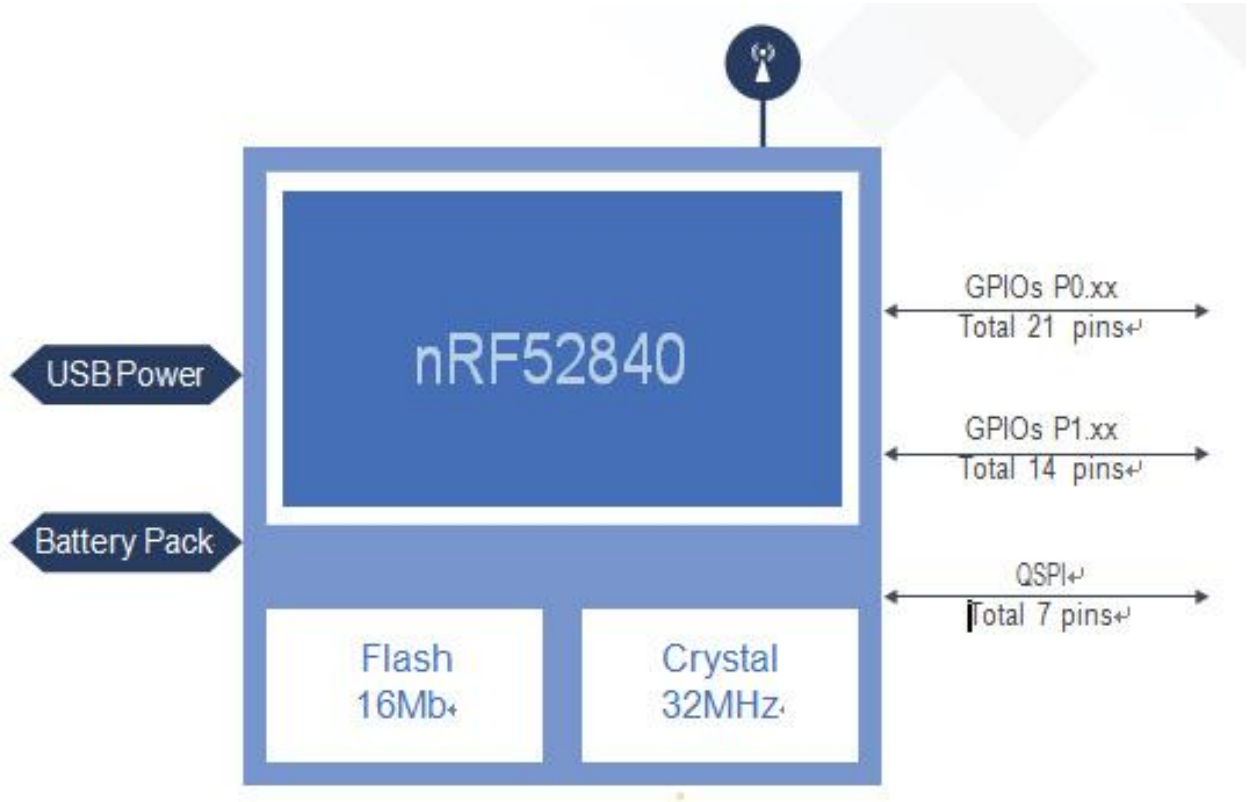
Single Power Supply Voltage

- Full voltage range: 2.7-3.6V

Detail Specification

Technical Specification	
MainChip	nRF52840
Bluetooth	5.0
Flash Memory	GD25Q16E
Interface	BT: UART/QSPI/I2C/GPIO
Package	LGA-82pin
Moisture Sensitivity Levels(MSL)	Level-3
Dimension	6.5 x 6.5 x 1.6mm(Max.)
Recommended Operation Conditions	
Operating Voltage(MainChip)	1.7 V to 3.6 V
Operating Voltage(Flash)	2.7 V to 3.6 V
Temperature	－30℃ ~ + 85℃
Humidity	Storage < 60% / Operation < 80%

2. BLOCK DIAGRAM



3. SiP PIN ASSIGNMENT

Pin Name

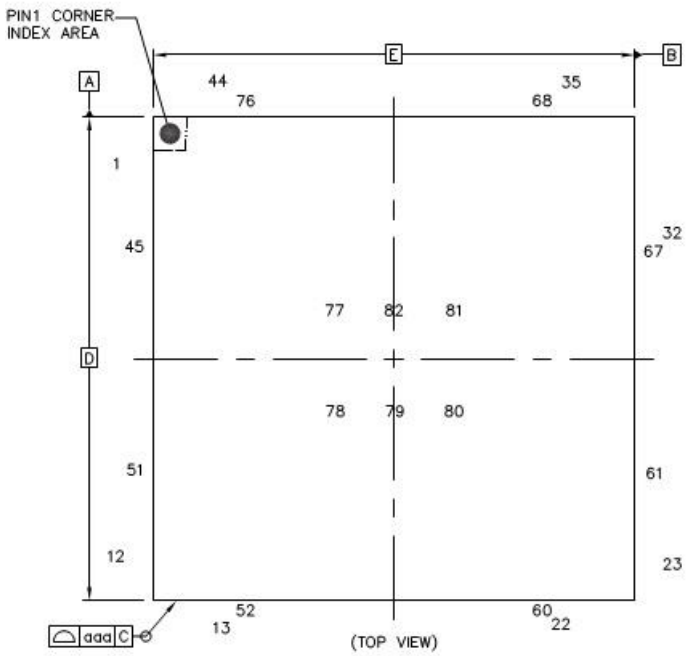
Pin #	Pin Name	Function	Description
1	P1.11	Digital I/O	General purpose I/O
2	P1.10	Digital I/O	General purpose I/O
3	P1.13	Digital I/O	General purpose I/O
4	P1.12	Digital I/O	General purpose I/O
5	VSS	Power	Ground
6	FR	ANT	Single-ended radio antenna connection
7	VSS	Power	Ground
8	P0.10 NFC2	Digital I/O NFC input	General purpose I/O NFC antenna connection
9	P0.09 NFC1	Digital I/O NFC input	General purpose I/O NFC antenna connection
10	VSS	Power	Ground
11	SWDCLK	Digital input	Serial wire debug clock input for debug and programming
12	SWDIO	Digital I/O	Serial wire debug I/O for debug and programming
13	P1.04	Digital I/O	General purpose I/O
14	FLASH_CS	Digital I/O	QSPI0_CS
15	FLASH_SIO2	Digital I/O	QSPI0_SIO2
16	FLASH_SIO1	Digital I/O	QSPI0_SIO1
17	FLASH_VCC	Power	Flash power 3.3V
18	FLASH_RSTN	Digital I/O	QSPI0_RSTN
19	FLASH_SIO3	Digital I/O	QSPI0_SIO3
20	FLASH_SIO0	Digital I/O	QSPI0_SIO0
21	FLASH_SCLK	Digital I/O	QSPI0_SCLK
22	DCCH	Power	DC/DC converter output
23	VBAT	NC	NC
24	VSS	Power	Ground
25	D+	USB	USB D+
26	D-	USB	USB D-
27	VSS	Power	Ground
28	P1.09 TRACEDATA3	Digital I/O Trace data	General purpose I/O Trace buffer TRACEDATA[3]
29	P1.08	Digital I/O	General purpose I/O
30	P0.13	Digital I/O	General purpose I/O

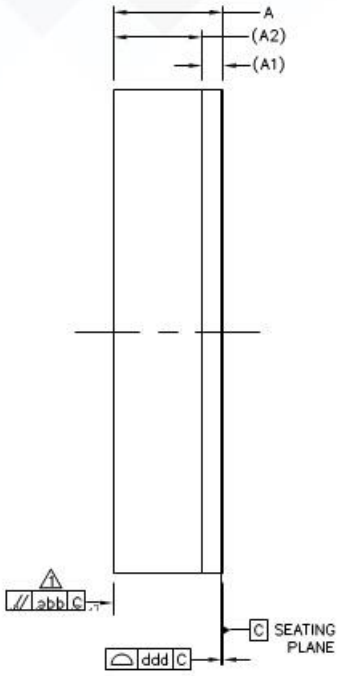
31	P0.14	Digital I/O	General purpose I/O
32	VSS	Power	Ground
33	P0.04 AIN2	Digital I/O Analog input	General purpose I/O Analog input
34	P0.05 AIN3	Digital I/O Analog input	General purpose I/O Analog input
35	P0.01 XL2	Digital I/O Analog input	General purpose I/O Connection for 32.768 kHz crystal
36	P0.00 XL1	Digital I/O Analog input	General purpose I/O Connection for 32.768 kHz crystal
37	VSS	Power	Ground
38	P0.27	Digital I/O	General purpose I/O
39	P0.30 AIN6	Digital I/O Analog input	General purpose I/O Analog input
40	P0.28 AIN4	Digital I/O Analog input	General purpose I/O Analog input
41	SW	NC	NC
42	NTC	NC	NC
43	PVSS	NC	NC
44	VSYS	NC	NC
45	P1.07	Digital I/O	General purpose I/O
46	P1.05	Digital I/O	General purpose I/O
47	P1.02	Digital I/O	General purpose I/O
48	P0.24	Digital I/O	General purpose I/O
49	P0.23	Digital I/O	General purpose I/O
50	P0.20	Digital I/O	General purpose I/O
51	P0.18 nRESET	Digital I/O	General purpose I/O Configurable as pin reset
52	P1.00 FLASH_CS_In	Digital I/O	General purpose I/O Connect with QSPI0_CS
53	P0.22 FLASH_SIO2_In	Digital I/O	General purpose I/O Connect with QSPI0_SIO2
54	P0.15 FLASH_SIO1_In	Digital I/O	General purpose I/O Connect with QSPI0_SIO1
55	FLASH_GND	Power	Flash Ground
56	P1.01 FLASH_RSTN_In	Digital I/O	General purpose I/O Connect with QSPI0_RSTN
57	P0.19	Digital I/O	General purpose I/O

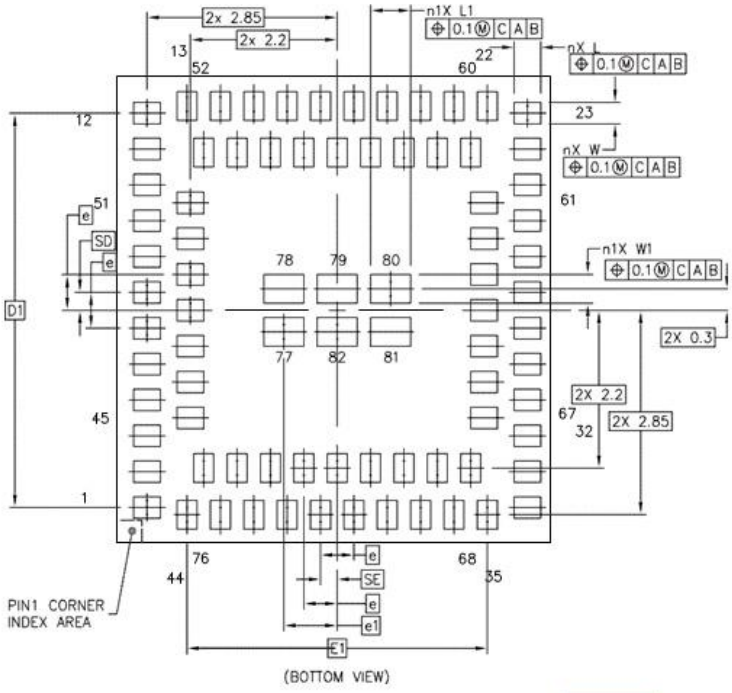
	FLASH_SIO3_In		Connect with QSPI0_SIO3
58	P0.21 FLASH_SIO0_In	Digital I/O	General purpose I/O Connect with QSPI0_SIO0
59	P0.25 FLASH_SCLK_In	Digital I/O	General purpose I/O Connect with QSPI0_SCLK
60	P0.12 TRACEDATA1	Digital I/O Trace data	General purpose I/O Trace buffer TRACEDATA[1]
61	P0.08	Digital I/O	General purpose I/O
62	P0.11 TRACEDATA2	Digital I/O Trace data	General purpose I/O Trace buffer TRACEDATA[2]
63	P0.07 TRACECLK	Digital I/O Trace clock	General purpose I/O Trace buffer clock
64	P0.06	Digital I/O	General purpose I/O
65	P0.16	Digital I/O	General purpose I/O
66	P0.17	Digital I/O	General purpose I/O
67	P0.26	Digital I/O	General purpose I/O
68	P0.31 AIN7	Digital I/O Analog input	General purpose I/O Analog input
69	P0.29 AIN5	Digital I/O Analog input	General purpose I/O Analog input
70	P0.03 AIN1	Digital I/O Analog input	General purpose I/O Analog input
71	P0.02 AIN0	Digital I/O Analog input	General purpose I/O Analog input
72	P1.15	Digital I/O	General purpose I/O
73	P1.14	Digital I/O	General purpose I/O
74	P1.03	Digital I/O	General purpose I/O
75	P1.06	Digital I/O	General purpose I/O
76	DEC5 NC	Power	1.3 V regulator supply decoupling for build codes Dxx and earlier. Not connected for build codes Fxx and later.
77	ICHG	NC	NC
78	VSS	Power	Ground
79	VBUS	Power	Input supply
80	VSS	Power	Ground
81	VDD_nRF	Power	Power supply 3.3V
82	VSS	Power	Ground

4. PACKAGE OUTLINE

Outline Dimension







	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	—	—	1.6
SUBSTRATE THICKNESS	A1		0.28	REF
MOLD THICKNESS	A2		1.2	REF
BODY SIZE	D		6.5	BSC
	E		6.5	BSC
LEAD WIDTH	W	0.25	0.3	0.35
LEAD LENGTH	L	0.35	0.4	0.45
LEAD WIDTH	W1	0.35	0.4	0.45
LEAD LENGTH	L1	0.55	0.6	0.65
LEAD PITCH	e		0.5	BSC
LEAD PITCH	e1		0.8	BSC
LEAD COUNT	n		76	
LEAD COUNT	n1		6	
EDGE LEAD CENTER TO CENTER	D1		5.5	BSC
	E1		4.5	BSC
BODY CENTER TO CONTACT LEAD	SD		0.25	BSC
	SE		0.25	BSC
PRE-SOLDER		—	—	—
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	

5. SPECIFICATION

Any technical spec shall refer to Nordic's official documents as final reference. Contents below are from " nRF52840 Product Specification v1.7 ".

Absolute Maximum Ratings

Note	Min.	Max.	Unit
Supply voltages			
VDD	-0.3	+3.6	V
VBUS	-0.3	+5.8	V
Flash_VCC		+3.6	V
I/O pin voltage			
VI/O, VDD ≤3.6 V	-0.3	VDD+0.3	V

Operating Conditions

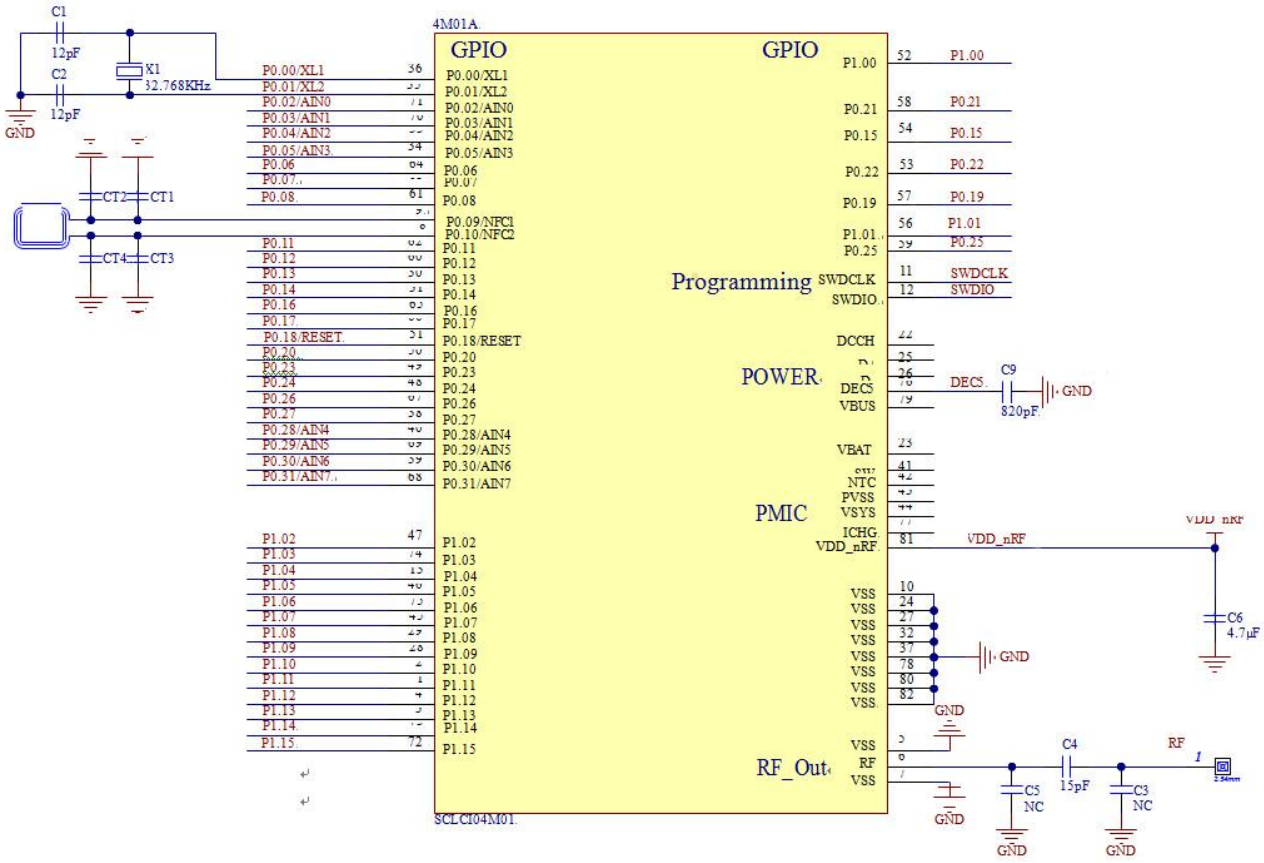
Symbol	Parameter	Min.	Min.	Nom.	Unit
VDD_nRF	VDD supply voltage	1.7	3.3	3.6	V
VDDPOR	VDD supply voltage needed during power-on reset	1.75			V
VBUS	VBUS USB supply voltage	4.4	5.0	5.5	V
Flash_VCC	Flash supply voltage	1.65	3.3	3.6	V
TR_VDD	Supply rise time (0 V to 1.7 V)			60.0	ms

6. REFERENCE DESIGN

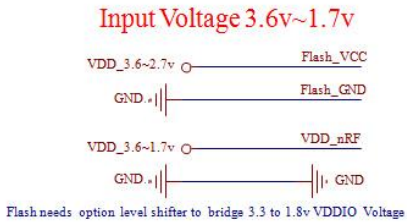
Before getting start:

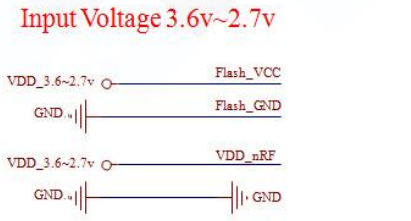
- Pin 81 VDD_nRF for the SiP power input 3.3V use.
- 32MHz crystal is already inside the SiP.
- When NOT using NFC, please remove ANT1 / CT1~CT4.
- When using internal 32.768KHz RC oscillator, please remove X1 / C2 / C3.

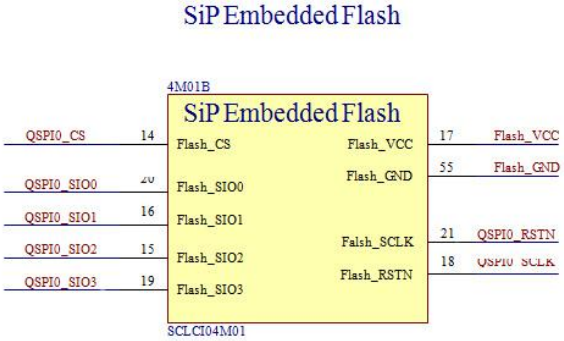
Reference Design

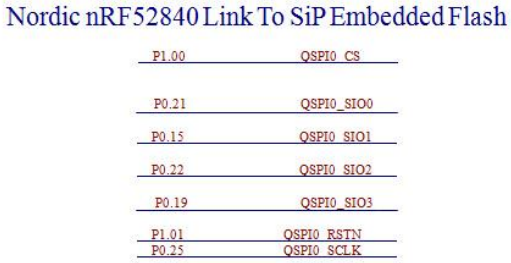


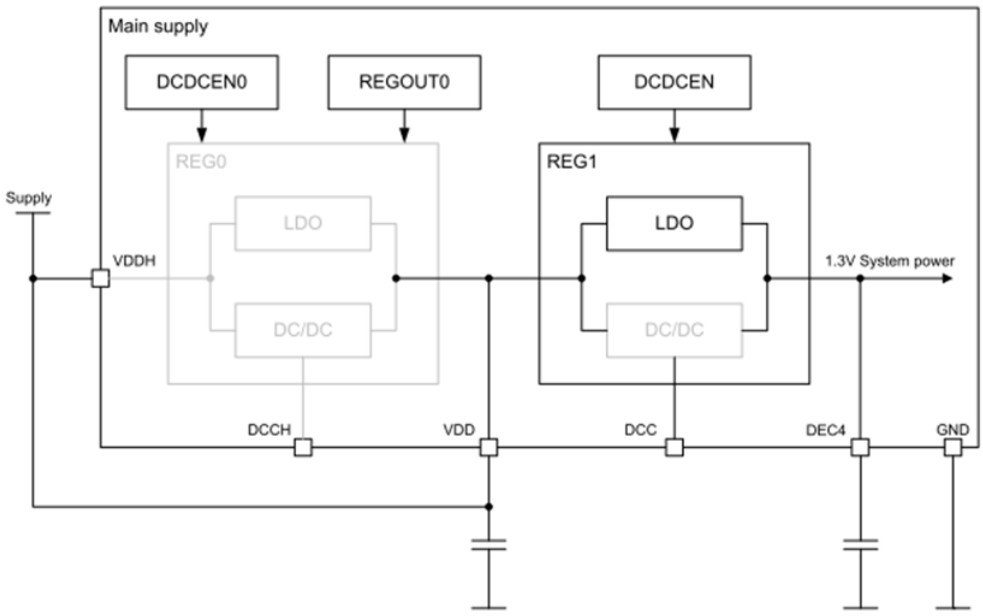
Reference Design











7. EMBEDDED FLASH STATUS REGISTER AND COMMAND

Flash technical spec shall refer to GigaDevice official documents . Contents below are from " GD25Q16E v1.2 ".

Status Register

Status Register-SR No.1

No.	Name	Description	Note
S7	SRP0	Status Register Protection Bit	Non-volatile writable
S6	BP4	Block Protect Bit	Non-volatile writable
S5	BP3	Block Protect Bit	Non-volatile writable
S4	BP2	Block Protect Bit	Non-volatile writable
S3	BP1	Block Protect Bit	Non-volatile writable
S2	BP0	Block Protect Bit	Non-volatile writable
S1	WEL	Write Enable Latch	Volatile, read only
S0	WIP	Erase/Write In Progress	Volatile, read only

Status Register-SR No.2

No.	Name	Description	Note
S15	SUS	Suspend Bit	Volatile, read only
S14	CMP	Complement Protect Bit	Non-volatile writable
S13	Reserved	Reserved	Reserved
S12	DC	Dummy Configuration Bit	Non-volatile writable
S11	LB1	Security Register Lock Bit	Non-volatile writable (OTP)
S10	LB0	Security Register Lock Bit	Non-volatile writable (OTP)
S9	QE	Quad Enable Bit	Non-volatile writable
S8	SRP1	Status Register Protection Bit	Non-volatile writable

Command Descriptions

Commands

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Write Enable	06H								
Write Disable	04H								
Read Status Register-1	05H	(S7-S0)	(cont.)						
Read Status Register-2	35H	(S15-S8)	(cont.)						
Write Status Register-1&2	01H	S7-S0	S15-S8						
Volatile SR write Enable	50H								
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(cont.)			
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)[1]	(cont.)		
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)[2]	(cont.)		
Dual I/O Fast Read	BBH	A23-A16[3]	A15-A8[3]	A7-A0[3]	M7-M0[4]	(D7-D0)[1]	(cont.)		
Quad I/O Fast Read	EBH	A23-A16[5]	A15-A8[5]	A7-A0[5]	M7-M0[6]	dummy	dummy	(D7-D0)[2]	(cont.)
Set Burst with Wrap	77H	dummy[7]	dummy[7]	dummy[7]	W7-W0[7]				
Page Program	02H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Quad Page Program	32H	A23-A16	A15-A8	A7-A0	D7-D0[8]	Next Byte			
Sector Erase	20H	A23-A16	A15-A8	A7-A0					
Block Erase (32K)	52H	A23-A16	A15-A8	A7-A0					
Block Erase (64K)	D8H	A23-A16	A15-A8	A7-A0					
Read Manufacturer/ Device ID	90H	00H	00H	00H	(MID7-MID0)	(ID7-ID0)	(cont.)		
Read Identification	9FH	(MID7-MID0)	(ID15-ID8)	(ID7-ID0)	(cont.)				
Read Unique ID	4BH	00H	00H	00H	dummy	(UID7-UID0)	(cont.)		
Erase Security Registers[9]	44H	A23-A16	A15-A8	A7-A0					
Program Security Registers[9]	42H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Read Security Registers[9]	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Enable Reset	66H								
Reset	99H								
Program/Erase Suspend	75H								
Program/Erase Resume	7AH								
Deep Power-Down	B9H								
Release From Deep Power-Down	ABH								
Release From Deep Power-Down and	ABH	dummy	dummy	dummy	(ID7-ID0)	(cont.)			

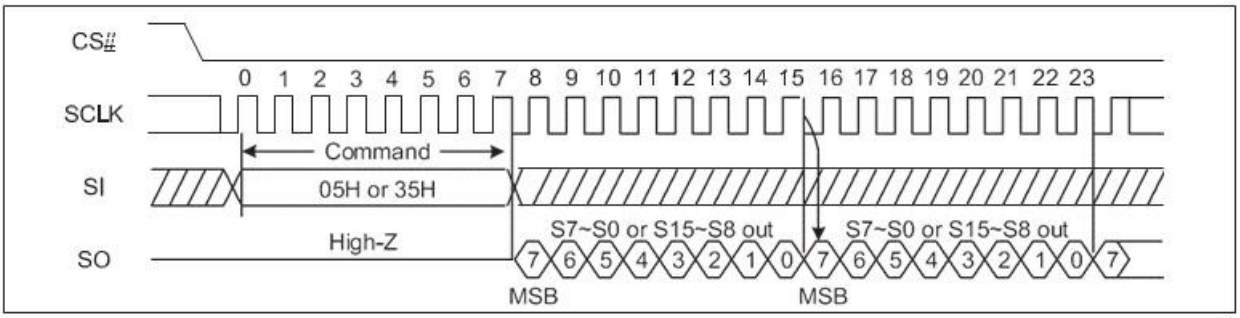
Read Device ID									
Read Serial Flash Discoverable Parameter	5AH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		

Note:

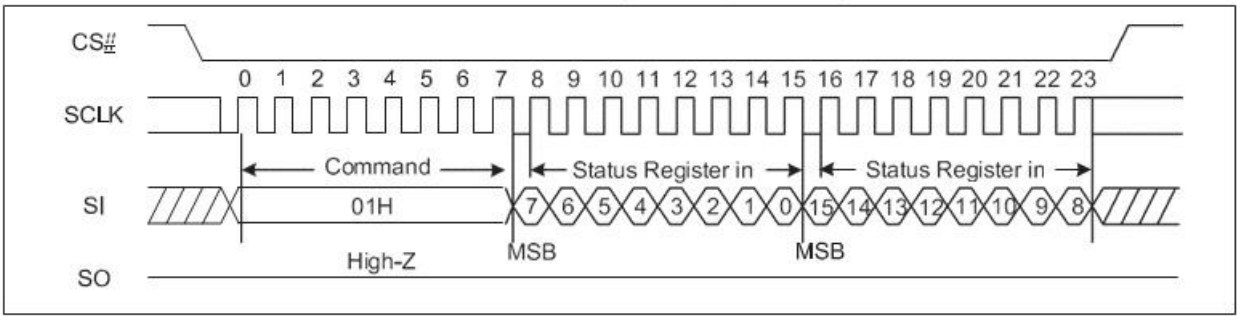
1. Dual Output data
IO0 = (D6, D4, D2, D0)
IO1 = (D7, D5, D3, D1)
2. Quad Output Data
IO0 = (D4, D0, …)
IO1 = (D5, D1, …)
IO2 = (D6, D2, …)
IO3 = (D7, D3, …)
3. Dual Input Address
IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0
IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1
4. Dual Input Mode bit
IO0 = M6, M4, M2, M0
IO1 = M7, M5, M3, M1
5. Quad Input Address
IO0 = A20, A16, A12, A8, A4, A0
IO1 = A21, A17, A13, A9, A5, A1
IO2 = A22, A18, A14, A10, A6, A2
IO3 = A23, A19, A15, A11, A7, A3
6. Quad Input
Mode bit IO0 = M4,
M0
IO1 = M5, M1
IO2 = M6, M2
IO3 = M7, M3
7. Dummy bits and Wrap Bits
IO0 = (x, x, x, x, x, x, W4, x)
IO1 = (x, x, x, x, x, x, W5, x)
IO2 = (x, x, x, x, x, x, W6, x)
IO3 = (x, x, x, x, x, x, x, x)
8. Quad Output
Data IO0 = D4, D0,
…
IO1 = D5, D1, …
IO2 = D6, D2, …
IO3 = D7, D3, …
9. Security Registers Address
Security Register0: A23-A16=00H, A15-A12=0H, A11-A10 = 00b, A9-A0= Byte Address;
Security Register1: A23-A16=00H, A15-A12=1H, A11-A10 = 00b, A9-A0= Byte Address;

Read/Write Status Register

Read Status Register Sequence Diagram

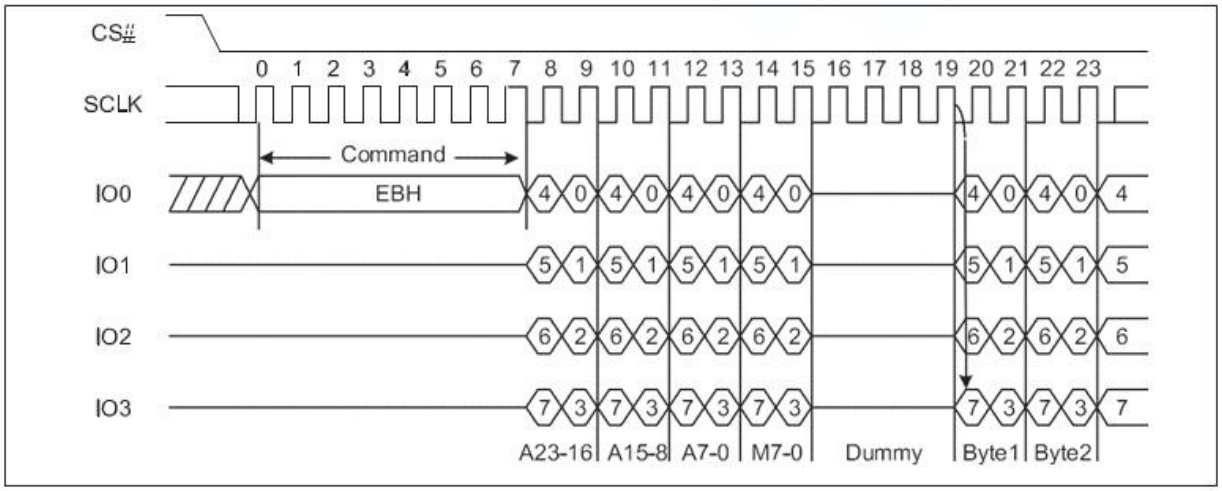


Write Status Register Sequence Diagram



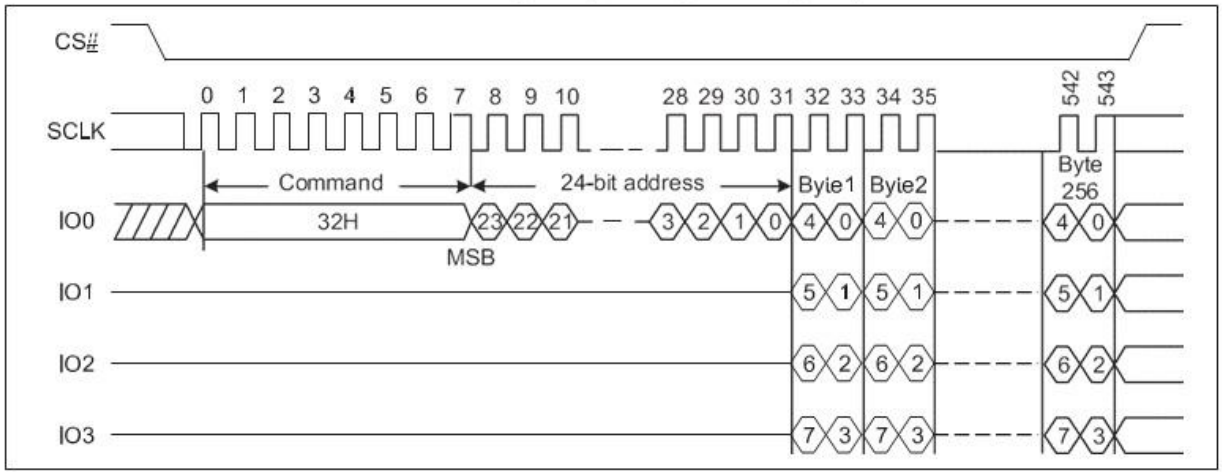
Quad I/O Fast Read

Quad I/O Fast Read Sequence Diagram ((M7-0) ≠ AXH)

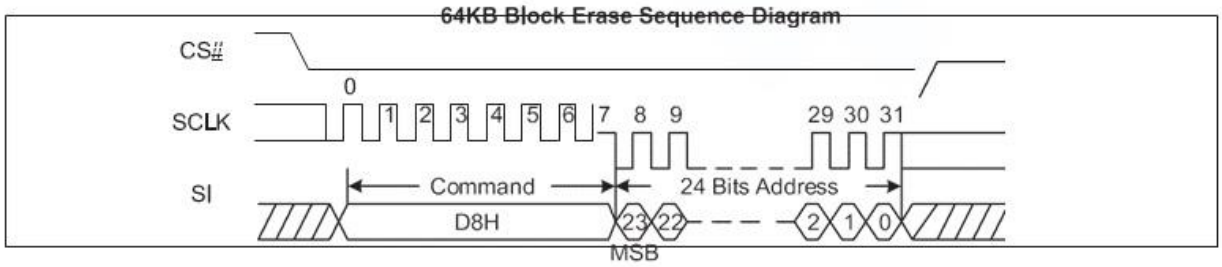


Quad Page Program

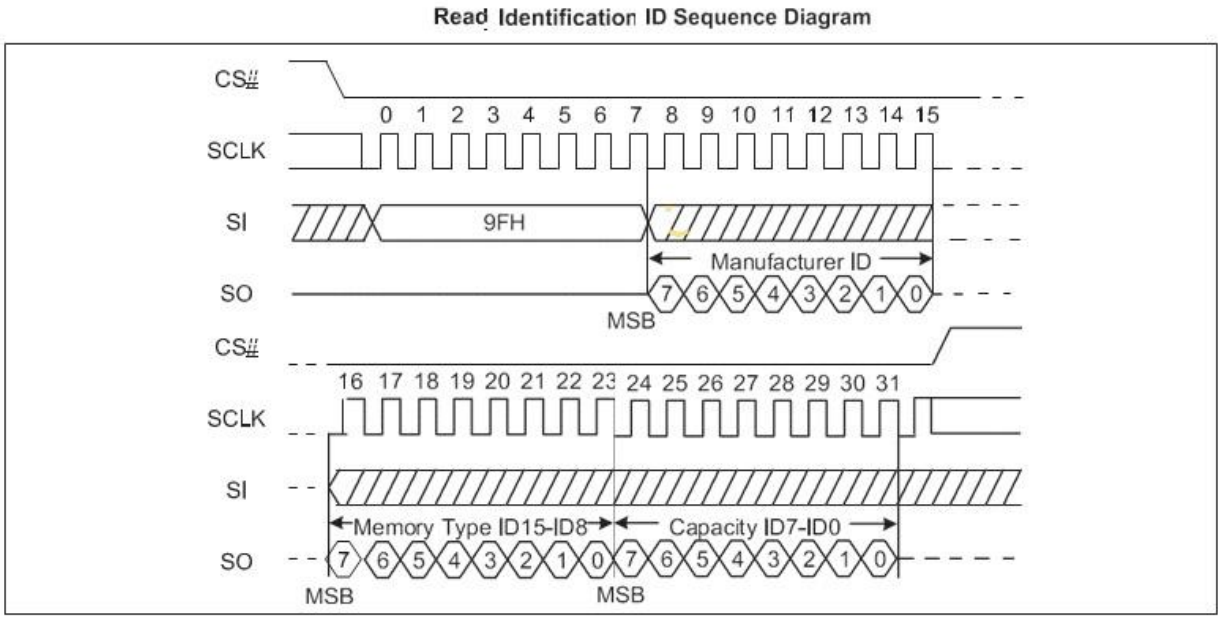
Quad Page Program Sequence Diagram



64KB Block Erase



Read Manufacture ID/Device ID



GD25Q16E

Operation Code	MID7-MID0	ID15-ID8	I D7-ID0
9FH	C8	40	15
90H	C8		14
ABH			14